ASIA & SOUTH PACIFIC INTERNATIONAL CONFERENCE ON EMBEDDED SoCs

(ASPICES 2005)

5-8 July 2005

A REPORT

ASPICES 2005 was the first International Conference on Embedded SoCs organized in the Indian Institute of Science, Bangalore during July 5-8, 2005.

Prof Gautam Barua, Director, IIT-Guwahati inaugurated the event and Prof P Balaram, Director, IISc presided.

Over 200 registered and invited delegates, both from India and abroad, attended the conference. A total of 9 invited state-of-the-art presentations by way of plenary and keynote talks were delivered by internationally acclaimed leaders in the field of embedded SoCs and a high quality technical program in which 22 papers were selected from a total of 112 submissions, of which, 9 papers were contributions from the universities and institutes in Japan and Taiwan. The remaining 13 papers were from universities/institutes in Europe, USA and India. The acceptance rate was little above 1 in 5.

10 papers that merited presentations in the conference, were presented as posters for want of sufficient time in the technical program.

15 sponsors for the conference made it possible to be uncompromising on the logistics and operations.

The highlight of the conference was the overwhelming response to tutorials totaling to 450 for 9 half day and 1 full day, that exceeded all our conservative estimates with the one on "Linux for Embedded Applications" making it a house-full+.

The four-day programme had tutorials on July 5 & 8 and conference on July 6 & 7.

Each of the above activities, summarized below:

JULY 5 – TUTORIAL – DAY 1:

The following half-day tutorials were conducted – 3 in the forenoon and 3 in the afternoon:

Tutorial – 1: Model Based Testing of Embedded Systems
Wolfgang Mueller, Paderborn University, Germany.

Model based methodologies became well recognized to deal with the increasing complexity in embedded systems and Systems-on-a-Chip design. In the context of model based testing, this tutorial gives an introduction to model based methodologies, languages, and tools.

In the first part of the tutorial, we briefly present the basic principles of the MDA (Model Driven Architecture) approach. MDA comes with the Unified Modelling Language (UML) and incorporates several principles of the platform based design. To derive test sequences from requirement specifications, we further present the classification tree methodology for embedded real-time systems (CTM/ES). CTM/ES identifies relevant system states and defines a sequence of test vectors for them. The second part of the tutorial gives an overview of currently applied test description languages and notations. We present UML 2.0 Sequence and Activitiy diagrams and their application to testbed definition. Thereafter, as a representative of a test definition language, we give an overview of ITU standard TTCN-3 followed by a brief introduction to the basic principles of temporal logic based property specification languages like PSL/Sugar.

The final part of the tutorial introduces tools for model based testing. There, we apply CTE (Classification Tree Editor) from Razorcat and AutomationDesk and MTest from DSPACE. The tools are introduced by examples from automotive design.

Tutorial – 2: Architecting a Heterogeneous Multiprocessor SoC Using a ULIW Template based Design Flow
Balakrishnan S, Philips Research Laboratories,The Netherlands

Current-day Systems on a Chip (SoCs) employ heterogeneous processing cores to address the high computation demands of streaming applications. Furthermore, solution providers for these applications often look for programmable cores for various reasons. To list a few, a programmable core can be reused in different products thereby amortizing the cost of the design effort. Also, programmable cores allow the solution provider to provide software upgrades to their products for better performance.

In this tutorial we will present the Ultra Long Instruction Word (ULIW) architecture template based design flow of Silicon Hive. We will first explain the rationale behind the architecture template while critically examining its generality. Next we will briefly examine the tools for describing the architecture, behavioural simulation of the algorithms, simulating the algorithms on the processor and generating RTL. Finally, taking an application as an example we will illustrate the architecting process of a SoC and expostulate the benefits of a C-based design flow.

Tutorial – 3: SOC Technology CMOS and Beyond
Navakanta Bhat, ECE Dept, IISc Bangalore

The CMOS technology in the sub-100nm regime is enabling the SOC integration. However, there are formidable challenges ahead in scaling the technolgy beyond 90nm node. The various issues in CMOS scaling will be discussed. Subsequently, the developments in intgrating MEMS sensors and actuators along with CMOS will be elaborated. The challenges in the design and fabrication of hybrid SOCs will be discussed with some case studies.

Tutorial – 4: Dynamically Reconfigurable Architectures for System Design
Kamal Aggarwal, Shridhar Laddha, Nachiket Urdhwareshe, SoftJin Infotech Pvt. Ltd, Bangalore

Reconfigurable architectures provide capability to dynamically 'change' the behavior of a hardware unit at run-time. The architecture can be configured to compute different tasks at different point of time. Such architectures offer significant benefits in terms of ASIC like performances (delay, power dissipation) for a given application (such as image processing) without the large costs associated with ASICs.

This tutorial would give a comprehensive view of the Reconfigurable architectures, application development and design tools for such architectures.

The tutorial is structured in three parts: in the first part we discuss the landscape of reconfigurable computing and try to classify various approaches. The second part discusses in detail a couple of dynamically reconfigurable processors using different programming paradigms. The third part deals with the tools' aspect, for the specific architectures.

Tutorial – 5: System Level Power Optimization
Bharadwaj Amrutur, ECE Dept, IISc Bangalore, India

This tutorial will cover techniques for optimizing the power consumption in modern VLSI systems. The tutorial will take a system level view of the problem and will cover all the layers in the system

design - semiconductor technology, circuits, microarchitecture, architecture, algorithms and application software. We will discuss the techniques applicable for power optimization at each layer. We will also highlight the trade-offs possible between power and performance at each layer of the system, both at design time and at run time. Examples from published literature will be used to explain the concepts.

Tutorial – 6: Visual Formalisms for Specification, Modeling and Verification of Embedded Systems
S. Ramesh and Ambar A. Gadkari, Indian Institute of Technology Bombay, Mumbai, India

Embedded systems comprise various interacting hardware and software components. With a high degree of system integration the development of hardware as well as embedded software demands design and verification methodologies leading to 'first-pass-successes'. Formal methods based on sound mathematical principles can provide effective solution to this problem. However, adoption of formal methods in practice poses difficulties due to unfriendly notations. Various attempts are being made to formalize the design and verification artifacts that are already used in practice or introduce the notations that are closer to those familiar to the practitioners; majority of which are visual and diagrammatic notations. This tutorial provides an overview of various such visual formalisms that exist, how these formalisms can be precisely interpreted and how the design and verification flows can be built around them.

JULY 6 – CONFERENCE – DAY 1:

PLENARY TALKS:

1. **FPGA Platforms, the Heart of Embedded Systems**
   Dr. Ivo Bolsens

During this presentation we will highlight the roadmap of programmable system platforms. We will discuss the opportunities and challenges of FPGA platforms and highlight the needs for future research in software tools to make design for FPGA a software experience rather than a tedious hardware design effort.

Providing the system design community with a field-programmable hardware platform that contains millions of gates, running at clock frequencies of several hundred MHz, communicating with immersed processors and distributed memories at GByte/s data rates is breaking down barriers to build tomorrows products.

These new platforms are creating new opportunities but also new challenges for the system design tool research that is trying to capture this ever growing design complexity and heterogeneity in new modeling languages, co-design flows, verification techniques and IP-re-use strategies.

Ivo Bolsens joined Xilinx in June 2001 as vice president and chief technology officer (CTO). He is responsible for identifying Xilinx technologies and talent as well as heading up the Xilinx Research Laboratories, which focus on advanced research in the area of programmable logic.

Mr. Bolsens came to Xilinx from the Belgium-based research center IMEC, where he was vice president research. He began there in 1984, holding various positions of increasing responsibility. His research included the development of tools for electrical verification for VLSI circuits, design of digital signal processing applications, and wireless communication terminals. He also headed the research on design technology for high level synthesis of DSP hardware, HW/SW co-design and system-on-chip design. This work lead to the creation of several start-up companies.

Bolsens earned his master's degree in electrical engineering and his Ph.D. in applied science from the Catholic University of Leuven in Belgium. He is author and co-author of more than 100 papers in the field of embedded system design, and wireless communication. He is also co-author of the book, "High Level Synthesis for Real Time Digital Signal Processing."

2. **Designing for Yield – New Insights**
   Dr. Vivek Sharma

The paper describes how by keeping the manufacturability and higher yield in focus while carrying out the VLSI design, can help in achieving better results in terms of yield and overall manufacturability. The presentation focuses on the key concepts and also certain design flow steps which can contribute to significant improvement in the final yields.

Vivek Sharma is the Director of STMicroelectronics in India. He is currently responsible for leading design groups in India involved in the creation of IPs, Systems-on-chip, Embedded Software and Application Software.

He has around 20 years of industrial experience and he moved to VLSI design in 1991 when he joined STMicroelectronics. In the initial years he pioneered Top Down Design Methodology for Mixed Analog designs and holds three patents. Since then, he has worked in various technical and managerial capacities and has played leadership role in building large design teams.

He graduated in Electronics and Communication engineering from Punjab Engineering College, Chandigarh and later on completed M. Tech. from Indian Institute of Technology, Delhi in communication engineering with thesis on Computer Networks."

KEYNOTE PRESENTATIONS:

1. **Paradigm Shift of SoC Design**
   Prof Satoshi Goto

Since LSI was invented 30 years ago, there was 3 big paradigm shift in the history of LSI design automation. The first one was happed in 1980 in physical design, the second one was in 1990 in logic design, and third one was happened in 2000 in high level design. In this talk, the design automation history is reviewed and predicted the next paradigm shift of design automation.

Satoshi Goto received the B.E. degree and the M.E. degree from Waseda University in 1968 and 1970, respectively. He also received the Dr. of Engineering from the same university in 1981. He joined Central Research Laboratories of NEC in 1970 and worked for NEC for 31 years until 2002. He was Vice President in charge of computer, software and networking research. After leaving NEC in 2002, he became Professor at Graduate School of Information, Production and Systems at Waseda University, Kitakyushu in April, 2003.

2. **Structured ASIC – A Disruptive Technology Promise**
   Dr. Mandalagiri Chandrasekhar

Rapid advances in semiconductor technology as predicted by Moore's law has resulted in shrinking the cost per transistor and enabled faster, cheaper, and more complex ASIC chips. One of the undesirable side effects has been the large increase in the cost of designing with standard cell ASIC, largely due to exponentially escalating cost of masks. Hence, the number of ASIC designs has decreased dramatically. FPGA technology on the other hand, which offers a standard off-the-shelf product with no upfront NRE costs has the disadvantage of higher unit costs, higher power consumption and lower performance compared to standard cell. A middle ground, that used to be the old gate array space, has recently emerged, aimed at combining the advantages of standard cell ASIC with those of FPGA. This relatively new market segment, referred to as Structured ASIC or Platform ASIC, still faces some major challenges. Numerous semiconductor and EDA vendors have jumped on the "Structured ASIC wagon", which started gaining strong momentum. However, a true

disruptive technology is required to answer the critical needs of today's consumer-oriented market and deliver on the Structured ASIC promise as envisioned by industry experts.

Mandalagiri Chandrasekhar is Director of Software Development at eASIC. During the last 20 years he has been involved in the development of EDA tools and chip design environments. He has held technical and management positions at Hewlett Packard Labs., in Palo Alto, Compass Design Automation, ViewLogic Systems and QuickLogic Corporation. He was instrumental in setting up the Bangalore operation of QuickLogic. He received his Bachelor's degree from Bangalore University, Masters Degree in ECE from the Indian Institute of Science, and PhD in Electrical Engineering from University of Southern California, Los Angeles.

3. **Next Generation Signalling Schemes for High-Bandwith Networking, Storage, Communication and Consumer Systems**
   Dr. Ramesh Senthinathan

Increases in demand for Internet access and content quality improvement, bandwidth requirements at all levels of the telecom chain are increasing explosively. System architects are confronted to build access management systems that can not only scale for future but also co-exist with legacy systems. Hence, in foreseeable future both electrical and optical networks will exist at different levels to meet the bandwidth demands. Presentation will focus on building silicon blocks to meet these requirements for high-speed/high-capacity router and switch designs. As the line cards move from 0.622G, 2.5G, and, 10G to 40G, state of the art electrical signaling schemes used to communicate between line (switch) cards are inadequate to keep par with these access speeds.

In addition to increase in speed, integration of large number of high-speed I/Os onto a single chip is essential for future switch and router designs. For example, a grooming switch with 144x 144 I/Os at 2.5 G would require each I/O to perform at six-sigma design to realize reasonable yield. Realization of such precision, high-density Giga core in CMOS requires innovative circuits design to overcome PVT variations as well as on-die variations. Designing signaling schemes from 0.622G to 2.5G would require new equalization techniques as well as advances in precision clock and data recovery design. Both transmitter pre-emphasis equalization and receiver equalization techniques and their advantages and disadvantages will be examined.

Supporting legacy systems requires one to solve crosstalk noise that is present in the connectors (limited by the height of shelve). Solving crosstalk at the speeds above 5G would require a paradigm shift in signaling scheme. Various research techniques to solve these problems will be presented. Finally the conversion between OEO and OOO networks and the challenges exist to push the OEO technology further will be discussed.

Ramesh Senthinathan received the B.S. degree in Computer Engineering from the State University of New York at Buffalo in 1984, and the M.S. and Ph.D. Degree in Electrical Engineering from the University of Arizona, Tucson in 1986 and 1992, respectively.

He was a Sr. Director of Engineering with Velio Communications (acquired by Rambus), Milpitas, CA, responsible for both technology and product development from 2001 to 2003. From 1995 to 2001, he was with Intel Corporation as a Director and Distinguished Engineer for the Microprocessor group in Folsom, CA. He was responsible for all aspects of circuit design of Pentium® Pro, and Pentium® III Microprocessor Design. From 1993 to 1995, he was with Motorola, Inc as a Principal Engineer responsible for 16/24 bit DSP analog and I/O circuit designs. He was a Staff Engineer with IBM Research from 1992 to 1993. From 1986 to 1989, he was a design Engineer with the ASIC and Microcontroller groups at Intel Corporation, Chandler, AZ.

Published more than 60 refereed papers, holds 6 U.S. patents, and is an author of the book "*Simultaneous Switching Noise of CMOS Devices and Systems*".

The papers presented in parallel sessions were 4 each in the areas of "Design Methodologies for SoC Platforms" and "Architecture Optimisations for Embedded Applications" and 3 in the area of "Design of Embedded SoC Applications", followed the Keynote Presentations in the respective sessions.

PANEL DISCUSSION:

The Panel Discussion was chaired by Prof N Balakrishnan, Chairman – Division of Information Technology, IISc.

With the panel discussion, technical programme for the day concluded.

CULTURAL PROGRAMME & BANQUET DINNER:

The banquet evening was unique in the ambience of the Cottage Industries Exposition and the musical rendering by Dr. Krishna Raghavendra from RARE.

JULY 7 – CONFERENCE – DAY 2:

PLENARY TALK:

Ensuring the Integrity of Power-Managed Designs
Dr. V. Visvanathan

The market demand for complex applications in portable devices has led to on-chip power management of high performance devices as the top-most design challenge in the sub-100-nanometer era. While a plethora of design techniques are available to minimize both active and stand-by power, the key CAD challenge is in verifying the signal and power integrity of a chip employing these techniques. The talk will describe various approaches to address this challenge and thereby ensuring first-pass silicon success.

V. Visvanathan is currently a Distinguished Member of the Technical Staff and Chief Technologist - ASIC, at Texas Instruments, India. His more than twenty years of professional experience is split roughly equally between Industry and Academia. He has previously been on the faculty of the University of Maryland, College Park and the Indian Institute of Science Bangalore. He has also worked at Bell Labs, Murray Hill, NJ, where he received the Distinguished Technical Staff award in 1989. He has more than fifty refereed conference and journal publications on various aspects of VLSI Design and CAD. His current area of work is on System-on-chip Design Flows and Methodologies. He holds a B.Tech from IIT Delhi and a Ph. D. from the University of California, Berkeley.

KEYNOTE PRESENTATIONS:

1. **High-end SoC Technologies and CAD Challenges**
   Nachiket Urdhwareshe

Various technological advances are enabling design and implementation of complex and high performance SoCs. However, there are specific CAD challenges being posed due to these technologies. This talk would discuss issues related to some of these technologies (more specifically, Dynamically reconfigurable architectures, Structured ASICs, DFM/DFY issues) in the context of

CAD approaches. All these technologies indicate need for *customized* CAD tool development. The talk would also underline the need of in-house CAD development activities within semiconductor companies in view of these technological advancements.

Nachiket Urdhwareshe is CEO of SoftJin, an EDA tool development services company based in Bangalore, India. In his 13 years of EDA industry experience, Nachiket has been involved in numerous CAD tool development engagements with semiconductor companies developing unique SoC technologies. Nachiket holds a Masters degree in Computer Science from Indian Institute of Technology, Mumbai.

2. **Shift in Design Paradigm – from Hardware Driven Design to Software Driven Design Paradigm for Multi-core SoC Design**
   Dr. Eshel Haritan

The fast digital life style, where people need to be connected anywhere and anytime, is enabled by convergent products that integrate computing and communication applications into a single portable consumer device. To meet the low power, low size, low cost and wireless connectivity requirements, these devices need to integrate very complex algorithms into a Systems-on-Chip (SoC). Design complexity, time-to-market pressure, and the flexibility required to evolve with emerging standards, are causing the design paradigm to shift from "Hardware Synthesis Driven Design" to "Software Driven Design". Instead of synthesizing algorithms in hardware, they are compiled as software on multi-processor SoC's. This approach provides a significant productivity and flexibility improvement over hardware design, provided:

- Software can be developed before the hardware is available
- Algorithm to multi-processor software mapping tools and methodologies become a reality

Eshel Haritan is vice president of engineering at CoWare. He joined CoWare as part of the recent alliance agreement with Cadence in September 2003. Eshel joined the Alta Group of Cadence in 1996. At Cadence, he managed the SPW product line engineering, and since January 2000, he managed the Cadence System-Level Design group engineering, including SPW, VCC, NC-SystemC and Test Builder. He joined Motorola Semiconductors Israel in 1985 and for more than 10 years developed layout, synthesis and simulation tools for internal use.

3. **A Multi-pronged Approach to achieving Low Power Designs**
   Dr. John Harrington.

Semiconductor devices have quickly grown beyond their original roots in the computing and communication environment to the vastly expanding consumer electronics market. This market has driven a number of new requirements and challenges to properly serve this customer segment. In addition to the obvious needs for low cost, low power consumption is now emerging as a primary requirement for silicon chips that are being designed for this market.

In order to meet these low power requirements head on, a number of techniques need to be pursued that go beyond just circuit design tricks; it also involves careful process selection and leveraging CAD automation to really squeeze the power out of the design. This talk will explore a number of avenues that are being pursued in the quest to get the maximum battery life while maintaining sufficient performance to meet the needs of the exploding consumer market.

John Harrington is currently Director of SoC and Serial I/O Development within the Storage Business Unit in Agere Systems, Allentown, PA. In his 25 years experience in the semiconductor industry, he has held numerous positions in general management, engineering management, and IC design. He holds a BSEE from Rensselaer Polytechnic Institute and an MSEE from Stanford University.

The papers presented in parallel sessions were 4 each in the areas of "Security Processors & Secure Computations" and "Reconfigurable Embedded SoC Platform for Content Application" and 3 in the area of "Design of Embedded SoC Applications" followed the Keynote Presentations in the respective sessions.

INDUSTRY WATCH:

The Industry Watch that was chaired by Prof H P Khincha, Chairman – Electrical Sciences Division, IISc, took the pride of place for the afternoon session.

With the industry watch session, the conference concluded.

JULY 8 – TUTORIAL – DAY 2:

Tutorial – 7: Linux for Embedded Applications
Darshak Vasavada, AllGo Embedded Systems, Bangalore

As embedded systems are becoming more and more powerful, more and more functionalities are expected from an embedded operating system, such as multi-tasking, networking, device drivers and user interface. Since these functionalities are already available in a desktop Linux, people often find it easier to port Linux on embedded systems, rather than adding new functionalities into an embedded kernel.

The main objective of this tutorial is to introduce Linux to an embedded system developer. The tutorial provides an overview of the Linux architecture and describes how to develop an embedded Linux system. In the second half, the tutorial discusses two variants of embedded Linux, viz., real-time Linux and micro-controller Linux.

The tutorial is divided into 4 modules as described below:

Overview of Linux kernel architecture: System call interface; Process management; Memory management; File system structure; Networking; Device driver structure.

Embedded Linux: Embedded Linux distributions and the Linux tool-chain; Linux boot loader; Building embedded Linux kernel; Developing embedded applications; Embedded shell; Developing device drivers.

Linux for real-time applications: requirements for real-time performance; interrupt latency; real-time scheduling; threads; enhancing device driver performance.

Linux for micro-controllers: Running Linux on the processors without MMU; Impact of the absence of MMU on process management, memory management and I/O management.

Tutorial – 8: Winning Strategies and Practical Approaches to SoC Design
Nagi Naganathan, Jacob Daniel Agere Systems, Allentown, USA,
AVSS Prasad, Agere Systems, Bangalore

The advent of nanometer design process has enabled the integration of multi-million gates with a variety of functionality as a system-on-chip (SoC). Today's SoC-based designs consist of a large number of reusable Intellectual Property (both analog and digital), high performance embedded processors, DSP functions, large amount of memory and software. The demand for SoCs are fueled by a strong demand in consumer oriented products for hand held computing, multimedia and other

communication products creating a demand for digital convergence with the need to design complex ICs in six to nine month design cycles. The high level of integration in a complex SoC with a constant pressure to time-to market has introduced several challenges such as: System level design, hardware-software codesign, low power, high performance, functional verification, deep submicron implementation (DSM) and designer productivity.

The tutorial will present a comprehensive introduction to SoC design techniques, applications and challenges in various facets of the process. We will present an in-depth introduction to concepts with a holistic view to overcome the various challenges and present strategies with a practical approach to the key issues in the design of SoCs.

The tutorial is divided into four parts. In the first part, we will present an overview and give an in-depth introduction to concepts in SoC design technology. This will cover the motivation for SoC design, key design challenges, opportunities and examples of different design approaches. An overview of the system level design challenges, introduction to embedded systems will also be presented.

The second part of the tutorial will cover detailed design methodologies, processes and successful flows for SoCs. The major steps associated with various aspects towards the SoC designs which include system level design, embedded software and implementation will also be covered. A successful strategy requires a concise specification of requirements and mapping the requirements through the whole design process. We will present detailed examples on mapping the marketing/system/product requirements to the system design and implementation. We will also present a motivation for reuse and present techniques for successful reuse.

The third part of the tutorial will cover the various aspects of verification. As the SoC designs are growing larger and more complex, functional verification is becoming a major factor for the success of the design due to prohibitive costs of implementing in silicon. We will present the various approaches for successful verification and present the latest trends in assertion-based verification using System Verilog which is an important part of the SoC design and validation. We will also present a methodology for the coverage-driven verification.

The fourth part of the tutorial will cover various aspects of embedded software development. The digital convergence requires the best ideas to carry over from software to hardware and vice-versa and requires a good co-design methodology. We will also present the platform based approach to the design of embedded systems towards the design of complex SoCs. We will discuss examples of some popular commercial platforms.

Tutorial – 9: Engineering Complex SoCs Using Configurable Microprocessor Cores
Himanshu A. Sanghavi, Tensilica Inc. Santa Clara, California, USA

This tutorial outlines the major forces changing today's SOC design process, and introduces the concept of SOC design using configurable and extensible processors as a basic design fabric. It will illustrate how extensible processors can be used as building blocks that provide the flexibility of a programmable solution and the performance characteristics of a hardwired RTL based solution.

The tutorial teaches the essentials of extensible processor architecture, tools for instruction-set extension, and multiple-processor SOC architecture for embedded systems. It covers topics such as efficient mapping of traditional hardware functions into application-specific processors, communication and synchronization between multiple processors, interfaces between processors and remaining hardware blocks and reducing power dissipation in processor-centric SOC designs.

The tutorial uses examples from Tensilica's Xtensa architecture and the Tensilica Instruction Extension (TIE) language throughout the presentation to give a precise and practical picture of the

issues and opportunities associated with this new design method. We will also present quantitative data obtained by applying this design methodology to several applications and industry standard benchmarks.

This tutorial is based in large part on Dr. Chris Rowen's recently published book, "Engineering the Complex SOC", Prentice Hall, 2004.

Tutorial – 10: Design of royalty free embedded processors using LISA
Dr. Andreas Hoffmann, CoWare Inc., Aachen, Germany
Sanjay Chakravarty, CoWare Private Ltd, Noida

The tutorial will start from a sample 32bit RISC architecture specified in the LISA 2.0 processor description language. Based on this sample model, a complete set of SW development tools including C-Compiler, ISS, Debugger as well as synthesizable RTL code can be automatically generated. The target application C-code is compiled and run on this processor – the students will then optimize the processor based on a successive process of profiling an algorithm and the architecture and changing the processor model based on these profiling results. We are expecting to see various architecture modifications, which support the algorithm under investigation most efficiently – from algorithm specific instructions to highly specialized SIMD (single instruction, multiple data) instructions for particular hot-spots. The instruction and micro-architecture design space is not restricted to simple extensions due to the language based nature of the CoWare LISATek Processor Design tool chain.

LOGISTICS:

The Chairmen & Staff of the Departments of CEDT and CADL at IISc provided the space for the Secretariat and resource support.

Web access and credit card payments for registration, travel, and hotel bookings brought in the desired flexibility in operations.

The team of volunteers from among the students of IISc provided the complementary and endless ubiquitous support for the event.

Prof S.K. Nandy	Prof. S.K. Sinha	Prof. H.S. Jamadagni
General Chair	Organizing Committee Chair	Industry Chair